col. 13, lines 12-61. The dual damascene structure of Yau et al. includes a substrate (712), a first intermetal dielectric layer (710), a first low k adhesive layer (714), a conventional silicon oxide or silicon nitride etch stop (716), a second low k adhesive layer (718), and a second intermetal dielectric layer (722). The stack is arranged as listed from bottom to top, and the first intermetal dielectric layer, the first low k adhesive layer, the etch stop, and the second low k adhesive layer are patterned and etched to receive contacts/vias. The second intermetal dielectric layer is etched to receive interconnects. Although not described by the specification, it appears in Figure 10F, 10G, and 10H, that the second low k adhesive layer (718) is patterned at the same width as the interconnect structure, and then replaced by a liner layer.

As described and illustrated by Applicants, the present invention, in independent claim 21, claims a multi-layer dielectric layer over a substrate for use in dual-damascene applications. The multi-layer dielectric layer includes a barrier layer disposed over the substrate, an inorganic dielectric layer disposed over the barrier layer, and a low dielectric constant layer disposed directly over the inorganic dielectric layer. The low dielectric constant layer is configured to receive metallization line trenches and the inorganic dielectric layer is configured to receive vias during a dual-damascene process.

In independent claim 31, Applicants claim a multi-layer inter-metal dielectric semiconductor structure. The multi-layer inter-metal dielectric semiconductor structure includes a barrier layer disposed over a base dielectric layer, an inorganic dielectric layer of an un-doped TEOS oxide disposed over the barrier layer, and a low dielectric constant layer of a carbon doped oxide disposed directly over the inorganic dielectric layer. The low dielectric constant layer is configured to receive metallization line trenches and the inorganic dielectric layer is configured to receive vias during a dual-damascene process.

In independent claim 36, Applicants claim a dielectric structure for dual-damascene applications. The dielectric structure includes a barrier disposed over a base dielectric, an inorganic dielectric layer of a fluorine doped oxide disposed over the barrier, and a low dielectric constant layer of a carbon doped oxide disposed directly over the inorganic dielectric layer. The low dielectric constant layer is configured to receive metallization line trenches and the inorganic dielectric layer is configured to receive vias during a dual-damascene process.

Finally, in independent claim 41, Applicants claim a multi-layer dielectric layer over a substrate for use in dual-damascene applications. The multi-layer dielectric layer includes a barrier layer disposed over the substrate, an inorganic dielectric layer of a fluorine doped oxide disposed over the barrier layer, and a low dielectric constant layer of a carbon doped oxide disposed directly over the inorganic dielectric layer. A thickness of the inorganic dielectric layer of a fluorine doped oxide is about 4500 Angstroms and is configured to receive vias, and a

thickness of the low dielectric constant layer of a carbon doped oxide is greater than the thickness of the inorganic dielectric layer of a fluorine doped oxide and is configured to receive metallization line trenches during a dual-damascene process.

To anticipate a claim, the reference must teach each and every element, either expressly or inherently, of the claim. See MPEP §2131. Applicants respectfully submit that the Yau et al. reference fails to teach each and every element of Applicants' independent claims 21, 36 and 41. Specifically, contrary to the assertion in paper No. 8, Yau et al. fail to teach a barrier layer disposed over the substrate, and fail to teach an low dielectric constant layer disposed directly over the inorganic dielectric layer, wherein the low dielectric constant layer is configured to receive metallization line trenches.

In paper No. 8, the Office asserts that Yau et al. teach a barrier layer disposed over the substrate at column 1, lines 50-60, column 2, lines 30-40, and Figure 10H, item 712, of the reference. Applicants respectfully disagree and request reconsideration. At column 1, lines 50-60 of the reference, Yau et al. teach liner layers to prevent diffusion of metals into low k dielectrics. "For example, many low k dielectric materials are porous and are preferably protected by liner layers to prevent diffusion of metals" (col. 1, lines 52-54). This is not a barrier over a substrate, but a liner within the fabricated features of low k dielectric layer(s). Even if a portion of a "liner" could be characterized to be initially over the substrate (e.g., at a bottom of a via prior to removal), this liner would fail to teach a next feature of Applicants' claims that an inorganic dielectric layer is disposed over the barrier layer. In the instance of a liner, it is a metal deposited into the feature over the liner, the liner serving to protect the low k dielectric in which the feature is defined as described above.

At column 2, lines 30-40, the reference teaches low k dielectric layers used as liner or cap layers. Again, liners are not disposed over the substrate, and neither are cap layers which, as is well known, are used to prevent diffusion of materials into porous material. Nothing about liner or cap layers teach or suggest a barrier disposed over a substrate.

Finally, item 712 of Figure 10H is a substrate and not a barrier. See col. 13, line 14 identifying substrate 712.

The reference fails to teach a barrier layer disposed over the substrate, and therefore fails to teach each and every feature of Applicants' claimed invention. Further, Applicants' note the reference fails to teach the low dielectric constant layer configured to receive metallization line trenches. As shown in Figures 10F-10H of the Yau et al. reference, the illustrated structure is fabricated with contact/via structures through the first dielectric (which can be an inorganic dielectric) layer 710, the first low k adhesive layer 714, and the etch stop layer 716. Interconnects (arguably equivalent to Applicants trenches) are fabricated through the second

dielectric layer 722, and as illustrated, through the second low k adhesive layer 718. Even though a feature for the fabrication of interconnects is fabricated into the second low k adhesive layer 718, it is not fabricated to receive the metal feature itself, but as illustrated is fabricated to receive a liner. Further, even if it were characterized as configured to receive the feature, it is not the low k dielectric constant layer claimed by the Applicants. Applicants are claiming a low k dielectric layer disposed directly over the inorganic dielectric layer. In the reference, the low k dielectric layer that is fabricated as described is over an etch stop which is over another low k dielectric adhesive layer. The reference fails to teach a low dielectric constant layer disposed directly over the inorganic dielectric layer wherein the low dielectric constant layer is configured to receive metallization line trenches.

The Yau et al. reference fails to teach each and every element of Applicants' claimed invention and therefore does not anticipate the claimed invention. Applicants respectfully submit independent claims 21, 36, and 41 are patentable under 35 U.S.C. §102(e) over Yau et al. Dependent claims 22-24, 26-30, and 37-40, each of which depend either directly or indirectly from one of independent claims 21, 36, and 41 are likewise patentable. Applicants respectfully request reconsideration, and that the §102 rejections be withdrawn.

Rejections under 35 U.S.C. §103

Claim 31-36 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yau et al. in view of Wolf (*Silicon Processing for the VLSI Era, Volume 1 - Process Technology*). Applicants respectfully traverse this rejection and request reconsideration.

The §103 rejection is essentially the same as the §102 rejections as described above, with the Wolf reference combined with the Yau et al. reference to teach the feature of the inorganic dielectric layer is an un-doped TEOS oxide (claim 31). Although not stated, it is assumed the Office intended to use the Wolf reference, as well, to teach the feature of the inorganic dielectric layer of a fluorine doped oxide (claim 36).

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references when combined must teach or suggest all the claim limitations. (MPEP §2143). Applicants respectfully submit the Office has failed to establish a prima facie case of obviousness.

As submitted above, the Yau et al. reference fails to teach each and every feature of Applicants' independent claims 31 and 36. Specifically, Yau et al. fail to teach a barrier layer disposed over the substrate, and fail to teach a low dielectric constant layer of a carbon doped oxide disposed directly over the inorganic dielectric layer wherein the low dielectric constant layer is configured to receive metallization line trenches. Whether or not the Wolf reference is combined with Yau et al., the references fail to teach or suggest all of the claim limitations, and therefore the Office has failed to establish a *prima facie* case of obviousness.

Applicants submit independent claims 31 and 36 are patentable over Yau et al. in view of Wolf. Dependent claims 32-35, each of which depend directly or indirectly from independent claim 31 are likewise patentable. Applicants respectfully request reconsideration, and that the §103 rejections be withdrawn.

Applicants respectfully submit that all of the pending claims are in a condition for allowance, and a notice of allowance is respectfully requested. If the Examiner has any questions concerning the present response, the Examiner is kindly requested to contact the undersigned at (408) 749-6900, ext. 6905. If any additional fees are due in connection with this filing, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM1P106D). A copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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